IMPROVEMENTS TO VOLTAGE SAG RIDE-THROUGH PERFORMANCE OF AC VARIABLE SPEED DRIVES

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Abstract

Voltage sags originating in ac supply systems can cause nuisance tripping of variable speed drives (VSDs) resulting in production loss and restarting delays. In ac VSDs having an uncontrolled rectifier front-end, the effects of voltage sags on the dc link causing dc under-voltage or ac over-current faults initiate the tripping. This paper suggests modifications in the control algorithm in order to improve the sag ride-through performance of ac VSDs. The proposed strategy recommends maintaining the dc link voltage constant at the nominal value during a sag by utilising two control modes, viz. (a) by recovering the kinetic energy available in the rotating mass at high motor speeds and (b) by recovering the magnetic field energy available in the motor winding inductances at low speeds. By combining these two modes, the VSD can be configured to have improved voltage sag ride-through perforamance at all speeds.

1. INTRODUCTION

Solid State AC Variable Speed Drives have already become an integral part of many process plants and their usage is on the rise in industrial, commercial and residential applications [1]. It is projected that, about 50-60% of the electrical energy generated will be processed by solid state power electronic devices by the year 2010 compared to the present day levels of 10-20% [2]. However, VSDs are vulnerable to voltage sags [3-4]. Voltage sag is a momentary reduction of voltage and is usually characterised by its magnitude and duration with typical values of magnitude between 0.1- 0.9 p.u. and duration ranging from 0.5 cycles to 1 minute [5-7]. Voltage sags are reported to be the most frequent cause of disrupted operations of many industrial processes [3].

This paper concentrates on AC VSDs with a three-stage topology (Fig. 1) viz., a diode bridge rectifier front-end, a dc link capacitor and a PWM inverter [3, 8-9].

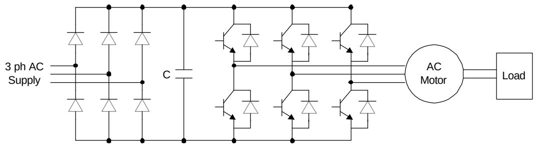


Figure 1. AC VSD with a VSI configuration

In VSDs having an uncontrolled rectifier front-end, variation in the incoming ac supply voltage is usually reflected in the dc link behaviour. In the case of a balanced three-phase sag, the dc link voltage reduces, leading to an under-voltage trip. Also when the ac supply returns to normal conditions, the VSD can trip due to the ac side over-current as a result of high charging current of the dc bus capacitor [3]. In the case of an unbalanced sag, the ripple in the dc bus voltage increases and the VSD can trip especially when the sag magnitude and the load torque are very high. It is reported that, a sag of magnitude more than 20% (i.e. ac voltage falls below 0.8 p.u.) and duration more than 12 cycles is found to trip VSDs [2]. The impact of unbalanced sag is less severe on the VSD performance and hence the ride-through behaviour when subjected to a balanced three-phase sag alone is analysed here.

2. CONVENTIONAL STRATEGIES

2.1 Types of available strategies

Three types of voltage sag mitigation techniques are reported in literature. They are, (a) hardware modifications (eg. increasing ac side inductors, dc bus capacitance) (b) improvement in power supply conditions (eg. use of alternative power supplies such as a motor-generator set, Uninterruptable Power Supply) and (c) modifying control algorithm. In this paper, strategies involving improvements in the control strategy alone are considered due to the following advantages, (a) no additional space is required and (b) since only software modifications are involved and hence cost increase is relatively negligible.

2.2 Control algorithm based strategies

One control algorithm based technique which ensures maximum torque availability to the motor suggests compensating the modulation index and stator frequency corresponding to the instantaneous dc link voltage during a sag [10]. However, the dc link characteristics are not improved and the drive can still trip when a sag occurs. Another strategy suggests maintaining the supply output of the VSD synchronised with the induction motor flux and operate the motor at zero slip during a sag so that the machine can be restarted when normal ac supply returns [9,11]. Since only a minimal power is drawn from the dc link, the rate of dc voltage reduction is low. However, the sag ride-through performance of the VSD depends on the dc link voltage at the instant of ac supply recovery. Finally, another control strategy recommends maintaining the dc bus voltage at a required level by recovering the kinetic energy available in the rotating mass during a sag [12]. With this type of control, the motor decelerates towards zero speed at a rate proportional to the amount of energy regenerated and the shaft load on the motor. But, since the kinetic energy decreases proportional to the square of the speed, the sag ride-through performance of the VSD under this strategy is highly speed dependent and it works well only at high motor speeds. If the voltage sag persists even after the motor has come to standstill, the capacitor voltage will start to reduce and the VSD will trip due to either under-voltage or over-current faults.

3. EFFECT OF VOLTAGE SAG ON AC VSDs

Here, the impact of a symmetrical three-phase sag on the VSDs controlling a synchronous reluctance motor (SRM) and an induction motor (IM) will be verified. Field orientation control (FOC) is considered. The VSDs were modeled in MATLAB^{TM} with details as discussed below.

3.1 Mathematical modeling of AC VSDs

In field oriented control of ac motors, the three phase motor currents are transformed into two orthogonal components in a synchronous frame of reference which moves with respect to the stator coordinates, and they are defined as i_{sq}, the torque producing component (quadrature axis current) and i_{sd}, the flux producing component (direct axis current) [13]. The main difference in the control of IMs as compared to the SRMs is due to the orientation of the flux axis. In the case of an SRM, the synchronous frame of reference is the same as the rotor axis, which can be kept track by a rotor position sensor whereas, in the case of IMs, more complicated computations are involved.

The functional block diagrams of SRM and IM VSDs under field orientation are shown in Figures 2 and 3 respectively. In both cases, the speed reference (W_{ref}) and the magnetising current reference (i_{mRref}) form the main control inputs. The operation of both VSDs is almost identical and the functions of various control blocks are as follows:

The Torque / Current Conversion block calculates the torque producing current set point (i_{sqset}) from the set torque reference (T_{ref}). The Current Control block calculates the stator voltage set points in field co-ordinates (V_{sdref} and V_{sqref}). The Co-ordinate Transformation block transforms the selected voltage references (V_{sdref} and V_{sqref}) from the synchronous co-ordinates to the stator co-ordinates. The Switching Vector Selection block selects the appropriate operating sequence for the inverter switches, based on the voltage vector position in the complex plane.

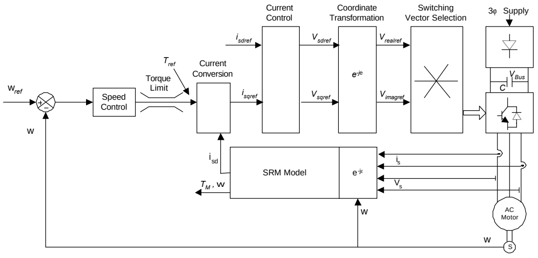


Figure 2 Functional block diagram of an SRM VSD

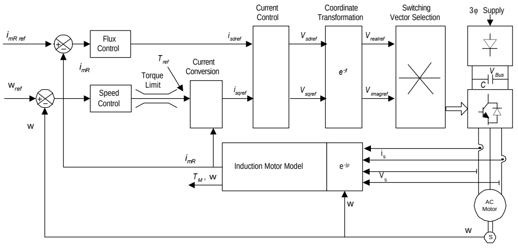
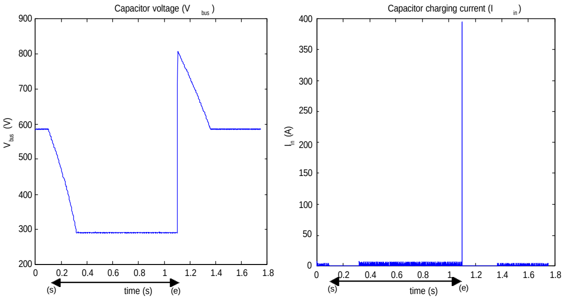


Figure 3 Functional block diagram of an IM VSD

3.2 Behaviour of VSDs on a sag condition

Here, the impact of voltage sag on the behaviour of both SRM and IM VSDs of 5.5 kW rating will be discussed. A symmetrical three-phase voltage sag of 0.5 p.u. and duration 1 second was applied when the motors were running at a steady-state speed of 120 rad/s operating with a load torque (T_L) of 18 Nm (half the rated load). The inverter switching frequency was kept at 5 kHz. The observations are as follows:

3.2.1 Behaviour of SRM VSD during a sag



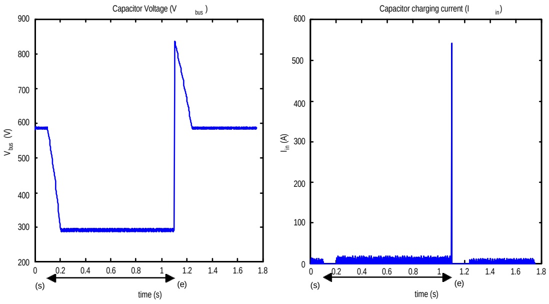
(a) (V_{bus}) (b) (I_{in})

Figure 4. DC bus characteristics of SRM VSD in the presence of a three-phase voltage sag

The control system has ensured that the SRM speed, torque and flux were unaffected during the sag condition. However, the dc bus characteristics, viz. the capacitor voltage (V_{bus}) and the capacitor charging current (I_{in}), are affected the most during the sag (Fig. 4). The double-ended arrow indicates the sag period.

It is observed from the above figures that initially there is no flow of capacitor charging current (I_{in}) because the rectifier diodes are reverse biased and the capacitor discharges the stored energy to the motor. Once V_{bus} becomes less than the ac supply peaks, the capacitor is charged uniformly by all the three phases during the sag. When the ac supply returns to normal, a very high current pulse is observed in I_{in} with its magnitude increasing with the sag magnitude, but it is usually many times the current rating of the rectifier diodes. This high current pulse results in the overshoot of V_{bus} which gradually returns to normal by discharging to the inverter load (Figure 4 (a)).

3.2.2 Behaviour of IM VSD during a sag



(a) V_{bus} (b) I_{in}

Figure 5. DC bus characteristics of IM VSD in the presence of a three-phase voltage sag

When subjected to the three-phase sag, the behaviour of the IM VSD was found to be identical to that of the SRM VSD. The speed and torque performances are not affected whereas the impact of the sag is observed in the dc link characteristics. The capacitor voltage (V_{bus}) and the capacitor charging current (I_{in}) are shown in Figures 5 (a) and (b) respectively.

3.3 Reasons for VSD tripping during a sag

From Figures 4 and 5, it can be observed that, the dc bus voltage reaches a low level depending on the magnitude of the sag and the load, which can cause the VSD to trip due to an under-voltage fault. When the sag condition is over, very high capacitor recharging current (I_{in}) results and in spite of being limited by the circuit impedances, it is usually several times the current handling capacity of the rectifier diodes. In such a case, the VSD can trip due to the over-current.

In order to protect the VSD hardware, the under-voltage trip setting is typically kept between 70% and 85% of the nominal dc voltage [11]. Similarly, the ac over-current trip is usually set in the range of 200% to 250% of the rated motor current.

4. PROPOSED CONTROL STRATEGY

Since the nuisance tripping of the VSD during a voltage sag is triggered by the dc bus characteristics, the proposed strategy, which is an extension of the control strategy proposed in [12], recommends maintaining the dc link voltage at the nominal level by recovering the kinetic as well as magnetic field energy present in the ac motor in order to improve the sag ride-through perforamnce.

4.1 Energy levels present in an ac VSD

The typical levels of energy present in an ac VSD controlling a 5.5 kW motor are given below:

Kinetic energy at rated speed = $\frac{1}{2} Jw^2 = 2835$ J (1)

Magnetising energy = $\frac{1}{2} LI^2 = 4.12$ J (2)

For a 5% ripple, the dc link capacitor C is chosen as 1000 μF, and

Energy stored in C = $\frac{1}{2} CV^2 = 172$ J (3)

4.2 Control sequence

From the numerical quantities given in Section 4.1 it is evident that there is a considerable amount of energy available in the rotating mass and a small amount in the winding inductances. Both these sources can be utilised to maintain the dc bus voltage at a desired level during a sag. Even though the available magnetisation energy is relatively small, once this energy is recovered, there will be no currents in the winding inductances and hence no energy drain from the link capacitor.

In order to establish an efficient and simple control system, it is better to attempt energy recovery from one source at a time. The fact that the motor requires magnetic field in order to function as a generator makes kinetic energy the first choice of energy source that can be recovered. When the motor functions as a generator, its speed falls more rapidly than normal coasting. When the motor speed reaches very low values, the stored kinetic energy reaches negligible proportions and the motor cannot deliver the energy required by the dc bus. There is no advantage in reducing the speed below some limit. Hence, a cut-off speed limit is defined (here 10% of the motor base speed) below which, this strategy would attempt to recover the energy available in the machine inductances.

4.3 Control Sequence and Flow-Charting

The flowchart illustrating the VSD control during a voltage sag condition is shown in Figure 6.

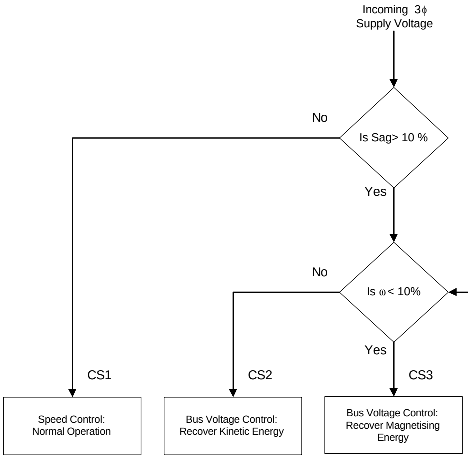


Figure 6. VSD control sequence during voltage sag condition

It can be observed that, there are three distinct situations involved with respect to the control of the VSD. They are summarised as follows:

Control Situation 1 (CS1): *(No Voltage sag)* VSD operation with normal speed control.

Control Situation 2 (CS2): *(Voltage sag and motor speed > cut-off speed)* DC bus voltage control by recovering load kinetic energy.

Control Situation 3 (CS3): *(Voltage sag and motor speed < cut-off speed)* DC bus voltage control by recovering magnetic field energy.

4.4 Proposed additional control loops

In order to maintain the dc link voltage at the required level during the sag, additional control loops are necessary within the VSD control system.

4.4.1 Kinetic energy recovery

Kinetic energy of the rotating mass can be recovered by operating the motor as a generator. Electrically this can be achieved by reversing the flow of energy from the ac motor to the dc bus by operating the motor at the rated flux. This operation is explained by the power balance equation (4).

$$V_{bus}\, I_{out} = \frac{2}{3}\,(V_{sd}\, i_{sd} + V_{sq}\, i_{sq}) \qquad (4)$$

where I_{out} is the dc output current.

From equation (4), it can be noted that, by maintaining the flux (i_{sd}) constant, if i_{sq} is reversed, the flow of the dc current I_{out} can be reversed from the motor to the dc bus which will boost the capacitor voltage. This is the basis of the control utilised in Control Situation 2.

In a sag condition, the recovery of kinetic energy must be controlled so that only the required amount of energy is recovered from the motor to maintain the capacitor voltage at the desired value. This can be achieved by the use of a closed loop PI controller, which monitors the capacitor voltage against the set reference and produces a suitable reverse torque reference. A new PI controller (Bus Voltage Controller 1) is configured in the VSD control system for this purpose. Figure 7 shows the sequence of operation of the control system during a sag at high motor speeds.

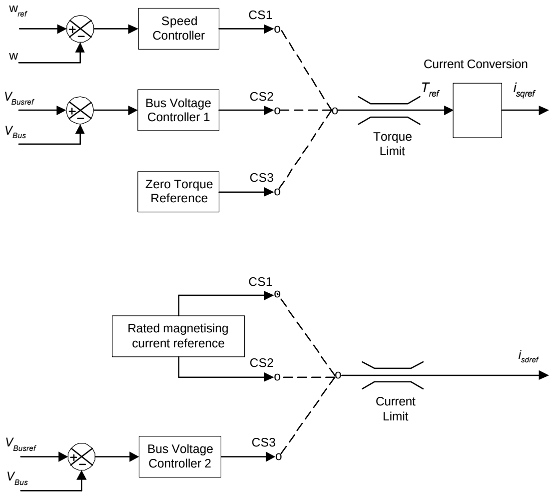


Figure 7 Control loops used to recover kinetic energy

Since the basis of speed and torque control operation is identical for IM and SRM VSDs, this control scheme is applicable in both the cases.

4.4.2 Magnetic field energy recovery

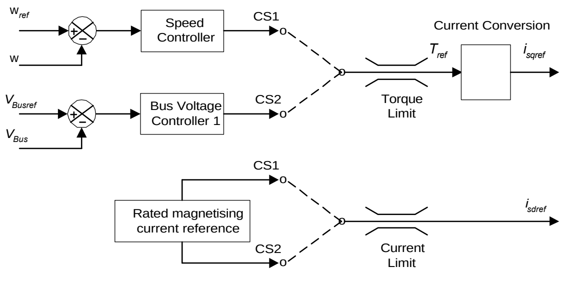


Figure 8 Control loops used to recover magnetic field energy

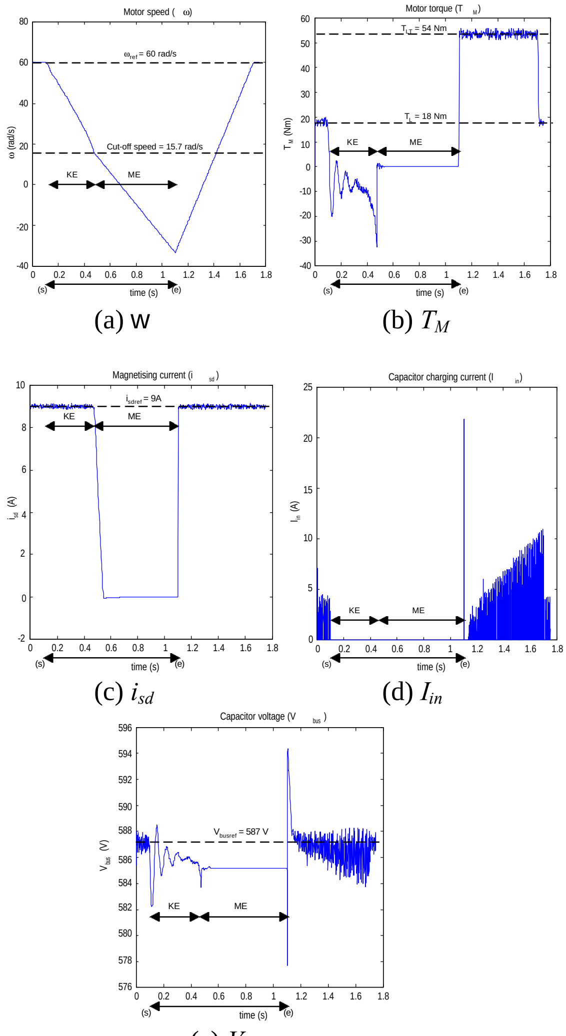
If a voltage sag occurs when the motor speed is below the cut-off limit (Control Situation 3), the magnetising energy stored in the motor inductances can be recovered to boost the bus capacitor voltage. This energy recovery can be achieved by lowering the magnetising current (which is i_{sd} for an SRM and

i_{mR} for an IM). There is no torque applied during this control situation (i.e. i_{sq} =0). From equation (4), it can be realised that this operation results in the reversal of flow of the current I_{out} from the motor to the dc bus, which will boost the capacitor voltage V_{bus}. In order to achieve a controlled recovery of this magnetising energy, another PI controller (Bus Voltage Controller 2) which monitors V_{bus} against the set reference is employed to control (reduce) the flux reference. Figure 8 shows the sequence of operation.

5. RESULTS

Above control strategies were implemented for a case where the VSDs were subjected to a 50% three-phase sag. Following sections illustrate the results. and the results are analysed as follows:

5.1 SRM VSD response



(a) w (b) T_M

(c) i_{sd} (d) I_{in}

(e) V_{bus}

Figure 9. Behaviour of SRM VSD during dc bus voltage control

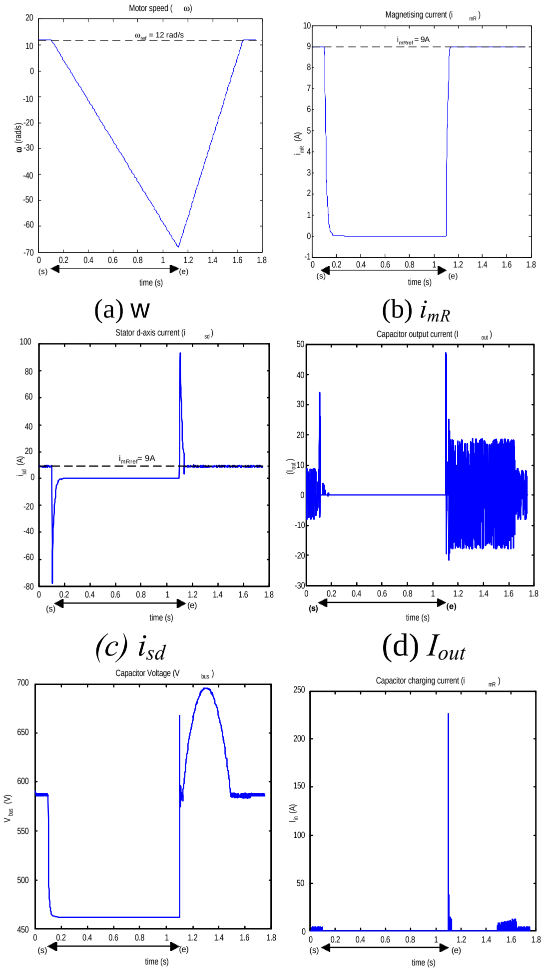
The voltage sag was applied to the SRM VSD when the motor was operating at a moderate speed of 60 rad/s. The characteristics of SRM speed (W), torque (T_M), magnetising current (i_{sd}), capacitor charging current (I_{in}) and the capacitor voltage (V_{bus}) are shown in Figure 9. The double-ended arrow indicates the sag condition and the kinetic and magnetising energy recovery periods are indicated as 'KE' and 'ME' respectively. It can be seen that the bus voltage is maintained at a level close to the set reference by initially recovering the kinetic energy as long as the motor speed is above the cut off speed and then by recovering the energy available in the inductances (by reducing i_{sd}). The motor speed is found to drop more rapidly due to the regenerative operation and then coast at a slower rate during the energy recovery from the motor windings. Oscillations are observed in the motor torque response because of the non-linear relationship between torque and the bus voltage, i.e. the torque requirement increases as the motor speed decreases. Once the supply returns to normal, the motor flux reaches its rated level and the motor starts to accelerate towards the set speed. The capacitor charging current (I_{in}) is found to be within acceptable limits on normal ac supply recovery.

5.2 IM VSD response

When controlled by the proposed strategy, the response of the IM VSD was found to be similar to that of SRM VSD at high motor speeds (i.e. Control Situation 2). The motor was controlled under regeneration mode and the dc link voltage was maintained around the set level (587 V). The motor speed was found to reduce towards zero. However, below the cut-off speed, while trying to recover energy from the winding inductances, the operation of the control system was found to be different from that of SRM. The observations and the analysis during Control Situation 3 are as given below:

5.2.1 Observations while recovering magnetisation energy

The response of the IM VSD, viz. speed (W), magnetisation current (i_{mR}), stator d-axis current (i_{sd}), capacitor output current to the inverter (I_{out}), capacitor voltage (V_{bus}) and the capacitor charging current (I_{in}) during the sag condition are shown in Figure 10. When the sag is sensed, the magnetising current (i_{mR}) is found to reduce to zero within a few milliseconds. When the motor flux decreases, a high negative current pulse (of about 80 A) is observed in i_{sd} characteristics. Also, it is observed that, the dc current I_{out}, instead of being fed back into the capacitor, has been drawn out of the capacitor by the motor. This has resulted in the reduction of capacitor voltage (V_{bus}) rather than being maintained at the set level. As a result, when normal ac supply returns, large current pulses are observed in the capacitor charging current (I_{in}). During the sag period, the motor speed is found to have coasted towards zero and reversed further which occurs only in the case of loads such as hoists or cranes whereas with frictional loads, the motor stops after reaching zero speed.



(a) ω (b) i_{mR}

(c) i_{sd} (d) I_{out}

(e) V_{bus} (f) I_{in}

Figure 10. IM VSD Response during attempted recovery of magnetising energy

At the end of the sag, the flux returns to normal rated value and the motor starts to accelerate towards the set speed. The motor operates in regeneration mode until the motor reaches zero speed and thereafter normal motoring operation starts. Because of this regeneration, the capacitor voltage V_{bus} is found to increase to a higher value than normal. This excess voltage can be controlled using the pre-charge resistors available in a standard VSD.

Obviously, it is clear from the simulation results that, the energy recovery from the magnetising inductances has not worked with an IM VSD and the reasons for this behaviour are analysed further.

5.2.2 Reasons for the inability to recover magnetising energy from IM

The stator and rotor currents of an induction motor in field co-ordinates are given as follows [13]:

$$i_{sd} = i_{mR} + T_R \frac{di_{mR}}{dt} \qquad (5)$$

$$di_{sd} = \frac{L_R}{R_R}\frac{di_{mR}}{dt} = L_m \frac{(1+\sigma_r)}{R_R}\frac{di_{mR}}{dt} \qquad (5(a))$$

$$i_{sq} = T_R i_{mR}(\omega_{mR} - \omega) = \frac{L_m(1+\sigma_r)}{R_R}(\omega_{mR} - \omega) \quad (6)$$

$$i_{rd} = -\frac{L_m}{R_R}\frac{di_{mR}}{dt} \qquad (7)$$

$$i_{rq} = -\frac{L_m i_{mR}}{R_R}(\omega_{mR} - \omega) \qquad (8)$$

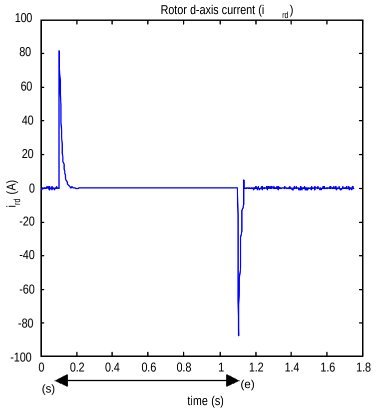


Figure 11. i_{sd} response during flux change

As per equation (5), the rotor flux of an induction motor (i_{mR}) is controlled by i_{sd}. During steady-state flux conditions, the average value of i_{sd} is the same as that of i_{mR}, but a little excess (d_{isd}), as given by equation (5(a)), is drawn from the dc bus. The corresponding energy is dissipated in the rotor circuit (compare equations (5(a)) and (7)). This is verified by the response of i_{sd} and i_{rd} (refer Figures 10(c) and 11). Again, it can be realised from equation (5) that, if the motor flux is reduced to zero in a duration shorter than the rotor time constant (T_R), i_{sd} would increase beyond its nominal level consuming more power from the dc link leading to a faster discharge of the dc bus capacitor. This explains the behaviour of the IM VSD during control situation CS3. Hence, during the sag, it is not a good idea to reduce the induction motor flux over a duration shorter than the rotor time constant.

An optimum dc bus voltage control can be achieved by reducing the flux to zero in a duration marginally longer than the rotor time constant and this can be achieved by an open loop flux control scheme. The advantage of this control is that, the energy drawn from the dc bus capacitor would be less than during constant flux control and would continue to reduce further. Hence, the dc bus voltage would reduce at a lower rate, which will enable the VSD to ride-through sags of longer durations at low motor speeds until zero speed.

6. CONCLUSIONS

The proposed strategy was found to work satisfactorily in the case of the SRM VSD. It was found that the dc link characteristics have improved and the VSD can ride through sags over a wide speed range. However, in the case of an IM VSD, it is observed that this strategy can override a sag only at high motor speeds. It was verified that the magnetic field energy gets dissipated across the rotor in the case of an IM. Thus, an open loop flux reduction at a rate higher than the rotor time constant will improve the sag ride-through performance of an IM VSD at low motor speeds.

The transition between various control loops during the different control situations was found to be smooth. The main advantage of this strategy is that the input rectifier is not in conduction during a voltage sag and hence the performance of the VSD is independent of the magnitude of the sag. Due to the same reason, the VSD load is decoupled from the mains and does not exacerbate the supply situation on the mains.

ACKNOWLEDGEMENTS

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